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Study of Electrical Performance of Hetero-Dielectric Gate Tunnel Field Effect Transistor (HDG TFET): A Novel Structure for Future Nanotechnology

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***Abstract* - Although, dynamic power in portable mobile devices can be reduced by reducing power supply V_{DD} on the cost of increased leakage current. Therefore, maintaining low leakage current in the device is serious issue for minimizing overall power consumption of the circuit and improving the battery life. The conventional Metal Oxide Field Effect Transistor (MOSFET) requires at least 60 mV of gate voltage for better current drive at room temperature which is difficult to achieve due to thermal limit. This limitation of gate voltage requirement degrades the performance of the device at lower V_{DD}. Tunnel Field Effect Transistor (TFET) is a potential candidate to replace CMOS in deep-submicron region due to its lower subthreshold slope SS (< 60 mV/decade) at room temperature. Steep switching in TFET can extend the supply voltage scaling with improved energy efficiency for both digital and analog applications. Despite those advantages, TFETs are suffering from lower ON current and larger ambipolar current. To overcome these shortcomings, a new structure, known as Hetero-dielectric gate TFET (HDG TFET), has been proposed in the literature. Since, in the absence of the compact analytical model, it is difficult to understand the electrical behaviour of the HDG TFET device, therefore, the present paper presents an analytical model of transconductance parameter of HDG TFET device. The electrical performance analysis of HDG TFET device reflects that on current can be increased considerably by choosing gate material of higher work function near the source region which also suppresses the ambipolar current. It is also observed that a thinner silicon film and larger drain bias result in larger transconductance value.**

Keywords—TFET, dynamic power, leakage current, transconductance, heterodielectric, surface potential

I. Introduction

Tunnel field effect transistor (TFET) has received attention of the researchers as an ideal alternative candidate to replace CMOS for design of nanoscale power efficient circuit due to its lower subthreshold swing (< 60 mV/decade) at room temperature [1-6]. But due to high tunneling resistance, on current in TFETs is much lower than the conventional MOSFETs. The larger ambipolar current in TFETs increases leakage power consumption. These two drawbacks of the TFET can be solved by employing heterodielectric gate instead of using single dielectric gate [7-9]. The proposed TFET structure is known as Hetro-dielectric gate TFET (HDGTFET). In this structure, the whole gate dielectric region is divided into two regions: region I near the source side which is occupied by larger dielectric gate material and region II near the drain side which is occupied by lower dielectric gate material [10-12]. The main purpose of placing high-κ oxide near the source to increase the on current due to local minima of conduction band edge of the tunneling junction whereas low-κ oxide near drain suppress the ambipolar current of the device. Apart from removing these two drawbacks, this structure also results in smaller SS than the conventional TFETs [13-14]. To sustain the scaling of MOS devices in future it is required to analyse these hetero-dielectric gate TFET in detail in terms of their electrical behaviour.

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In this paper, we have derived the analytical model of transconductance (g_m) parameter by utilizing our previously developed drain current model [15]. The electric filed distribution in the proposed structure is used to derive the tunneling generation rate which can be integrated to get the drain current model. Since, differentiating potential in the structure yields the 2D approach via Poisson equation in terms of surface potential and device electric field, therefore calculation of potential distribution is necessary for understanding the electrical behaviour of the device. The contribution of source/drain depletion width and quantum confinement effects have been ignored while deriving the models due to heavy doping and larger silicon film thickness (> 3 nm). The present paper is organized as: Section II describes analytical model of transconductance parameter. Section III discusses the electrical behaviour of the proposed structure and at the end, we conclude the paper in section IV.

II. Analytical Models

The transconductance (g_m) model of the proposed HDG TFET device is developed by using the drain current model. The process of formulation of drain current was based on integrating the BTBT generation which can be calculated by using electric field distribution in the proposed device. Differentiating potential (ψ) yields 2-D approach via Poisson equation in terms of surface potential and electric field distribution. The analytical model of the potential distribution in the present structure can be done by solving the 2-D Poisson's equation with parabolic approximation. The structure and coordinate system of the proposed N-type hetero-dielectric gate TFET (HDG TFET) is shown in Fig. 1 [15].

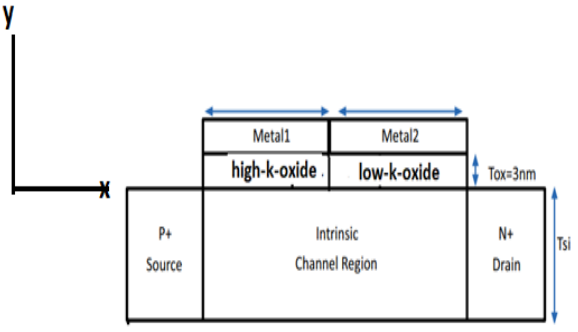

Fig. 1. Structure of HDGTFET.

After neglecting the fixed carrier oxide charges, 2-D Poisson's equation, for the potential distribution $\psi_j(x,y)$ in the respective region, is given as

$$\frac{d^2\psi_j(x,y)}{d^2x}+\frac{d^2\psi_j(x,y)}{d^2y}=-\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

, where N_a is the channel doping concentration, j = 1, 2 represents the region I and region II, ε_{si} is the silicon permittivity, $\psi_j(x, y)$ is the 2-D electrostatic potential in the region I and II measured with respect to Fermi potential. The solution of this differential Eq. (1) can be obtained by assuming parabolic profile along the film thickness t_{si}.

Following the same procedure, as mentioned in paper [16], the surface potential in the respective region is given as

$$\psi_{js}(x)=A_j e^{\frac{x-L_j}{\lambda_j}}+B_j e^{-\frac{x-L_j}{\lambda_j}}+\sigma_j \quad (2)$$

, where A_j and B_j are constant and determined using following Boundary Conditions (BCs):

$$\psi_{si}(x=0)=\upsilon_{bi1}$$
$$\psi_{si}(x=L_1)=\psi_{s_2}(x=L_1)$$
$$\frac{d\psi_{s1}(x=L_1)}{dx}=\frac{d\psi_{s_2}(x=L_1)}{dx}$$
$$\psi_{s_2}(x=2)=\upsilon_{bi2}+\upsilon_{ds}$$

, where υ_{bij} is the built-in-potential.

Using these boundary conditions (BCs) and after mathematical simplification, the values of the constants are [15]

$$A_1=\gamma_{11}+B_2 \quad , \quad B_1=-z_{12}B_2+z_{11} \quad , \quad A_2=\frac{\beta_{13}-\beta_{12}B_2}{\beta_{11}} \quad , \quad B_2=\frac{\beta_{14}}{\beta_{15}}$$

, where each constant has its own value as given in ref. [15].

Substituting the values of these constants in Eq. (2), the analytical expression of the channel potential can be determined and given as [15]

$$\psi_j(x,y)=\psi_{sj}(x)\left[\delta_{1j}+\delta_{4j}y^2\right]+\left[\delta_{2j}+\delta_{3j}y^2\right] \quad (3)$$

, where

$$\delta_{1j}=\frac{c_{ox_j}}{\varepsilon_{si}}\cdot\frac{t_{si}}{4}+1 \quad , \quad \delta_{2j}=\frac{c_{ox_j}}{\varepsilon_{si}}\cdot\frac{t_{si}}{4}V'_{GSF}$$
$$\delta_{3j}=\frac{-c_{ox_j}}{\varepsilon_{si}\ t_{si}}V'_{GSF} \quad , \quad \delta_{4j}=\frac{-c_{ox_j}}{\varepsilon_{si}\ t_{si}}$$

It is necessary to determine the tunneling width of the proposed structure to calculate the tunneling current from source-to-channel and ambipolar current from drain-channel. This parameter exhibits transition from strong dependence to weak dependence on the gate voltage [15].

$$x = (x_2 - x_1) = \frac{\lambda_1}{2}\{ln\frac{W_{14}}{2}\left(1 \pm \sqrt{1 - \frac{4W_{15}}{W_{14}}}\right) - ln\frac{W_{12}}{2}\left[1 \pm \sqrt{1 + \frac{W_{11}}{W_{12}^2}}\right]\} \quad (4)$$

, where $W_{11} = \frac{B_1}{A_1}e^{\frac{2L_1}{\lambda_1}}$, $W_{12} = \frac{A_1 + B_1 e^{\frac{2L_1}{\lambda_1}}}{A_1} - \frac{E_g}{q}$,

$W_{15} = \left(\frac{B_1}{A_1}\right)e^{\frac{2L_1}{\lambda_1}}$, $W_{14} = \left(\frac{\phi_{ch} + \frac{E_g}{q} - \sigma_1}{A_1}\right)e^{\frac{L_1}{\lambda_1}}$

and ϕ_{ch} is the channel potential.

In non-local BTBT, tunneling of charges start only when conduction band edge (CB) of source gets in line with the valence band edge (VB) of the channel region and the tunneling current can be obtained by integrating Kane's band-to-band tunneling (BTBT) generation rate over the entire tunneling volume in both radial and lateral directions as [15]. The analytical expression of tunneling current for the proposed structure is [15]

$$I_{BTBT(S-C)} = (q * W_{ch}) * (\frac{1}{\lambda_1}) * t_{si} * A_k * (\frac{E_g}{q})^1\{(A_1 * e^{-\frac{L_1}{\lambda_1}} - B_1 * e^{\frac{L_1}{\lambda_1}}) \ln\frac{x_2}{x_1} + (\lambda_{11} + \lambda_{12})(x_2 - x_1)\} \quad (5)$$

, A_k and B_k are Kane's parameters and their values are $A_k = 1.4 \times 10^{20}$ eV$^{1/2}$ cm.s.V^2 and $B_k = 8.6 \times 10^6$ V/cm.eV$^{3/2}$, respectively, t_{si} is film thickness, $\lambda_j = \sqrt{\frac{\varepsilon_{si} t_{si}}{2\varepsilon_{ox_j}}}$ is known as characteristic or scaling length and E_g is band gap of semiconductor material.

Transconductance (g_m) is the transfer characteristics of a device which displays the ability to amplify the signal and is defined as

$$\left[\frac{\partial I_{BTBT}}{\partial V_{GS}}\right] \quad \text{at constant } V_{DS} \quad (6)$$

For the proposed structure using Eq. (5) the analytical expression of the transconductance is

$$g_m = A_{11}[\left\{\frac{\partial A_1}{\partial V_{GS}}e^{-\frac{L_1}{\lambda_1}} - \frac{\partial B_1}{\partial V_{GS}}e^{\frac{L_1}{\lambda_1}}\right\}\ln\left(\frac{x_2}{x_1}\right) + \left(A_1 e^{-\frac{L_1}{\lambda_1}} - B_1 e^{\frac{L_1}{\lambda_1}}\right)\left(\frac{1}{x_2}\frac{\partial x_2}{\partial V_{GS}} - \frac{1}{x_1}\frac{\partial x_1}{\partial V_{GS}}\right) + (\lambda_{11} + \lambda_{12})\left(\frac{\partial x_2}{\partial V_{GS}} - \frac{\partial x_1}{\partial V_{GS}}\right)] \quad (7)$$

, where

$$A_{11} = \frac{qW_{ch}}{\lambda_1}t_{si}A_k(\frac{E_g}{q})$$

$$\frac{1}{\lambda_1} - \frac{q*B_k}{E_g} = \lambda_{11} \text{ and } \frac{1}{\lambda_1} + \frac{q*B_k}{E_g} = \lambda_{12}$$

III. RESULTS AND DISCUSSION

The developed analytical models are simulated in order to understand the electrical characteristics of the proposed device in detail. The values of various parameters used in the model are $L = 30$ nm, $L_1 = 15$-20 nm, $t_{si} = 5$ nm and $t_{ox} = 3$ nm, N_s (source concentration) $= 10^{20}$ cm^{-3}, N_d (drain concentration) $= 5 \times 10^{18}$ cm^{-3} and channel region concentration is 5×10^{15} cm^{-3}.

The developed analytical expression for tunneling width shows an excellent matching with 2-D ATLAS simulator results for larger permittivity in the source region as seen in Fig. 2(a). The analytical results also confirm that the higher dielectric permittivity near source reduces the tunneling width and accelerates the tunneling of carriers from source to channel.

ATLAS is a simulation package developed by SILVACO International [17] which is part of their TCAD framework. Atlas supports two and three-dimensional simulations. It solves Poisson's equation, the carrier continuity equations, and the lattice heat equation. Steady state, transient, AC-small signal and optical device simulation can be performed.

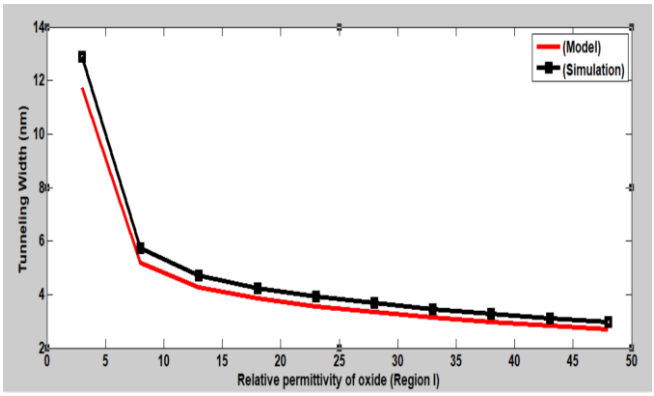

Fig. 2(a). Comparison of tunneling width of the proposed structure with 2-D Simulator result.

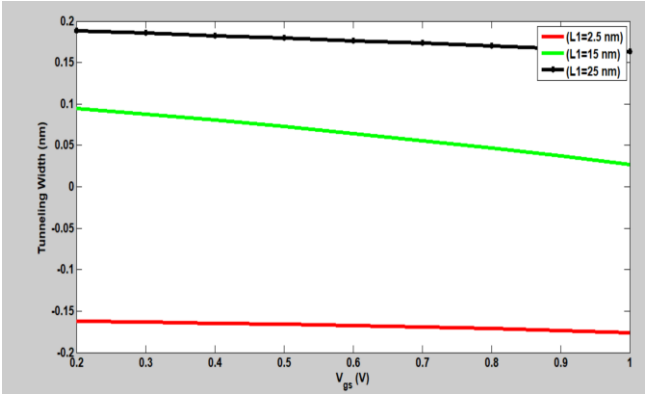

Fig. 2(b). Variation of tunneling width with gate source voltage for different L_1.

Figure 2(b) shows that the tunneling width becomes narrower when the structure of length L = 30 nm is equally divided into two regions which are occupied by larger dielectric material near source and SiO_2 dielectric material near drain side. This confirms our choice of L_1 = 15 nm.

The main purpose of choosing HDSG TFET is to increase ON current and reduce ambipolar current in the device. This can be achieved by lowering the surface potential near source-channel junction and higher surface potential near drain-channel junction. From Fig. 3 it is observed that by choosing gate material of larger work function near drain compared to the source channel junction. This study suggests that combining the gate engineering with material engineering, we can remove the two associated drawbacks of the conventional TFET.

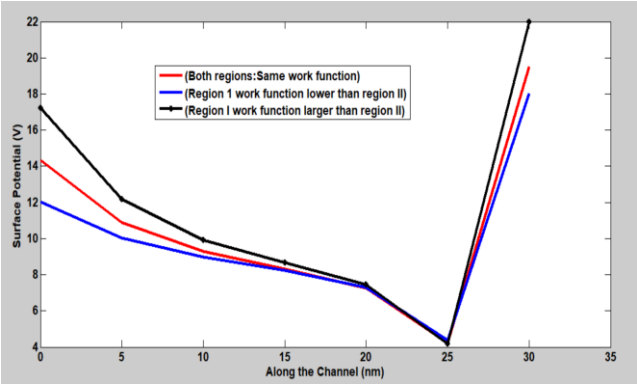

Fig. 3. Variation of surface potential along the channel for different combination of work function.

Figure 4 shows the variation of off current (ambipolar current) in the proposed device with film thickness (t_{si}) for different dielectric material in region I. It is observed that off current first decreases with t_{si} and later increases with thickness. It is observed that for dielectric material of strength k_{r1} = 50 and $t_{si} \geq 9$ nm we can get lower off current due to higher potential barrier near the drain.

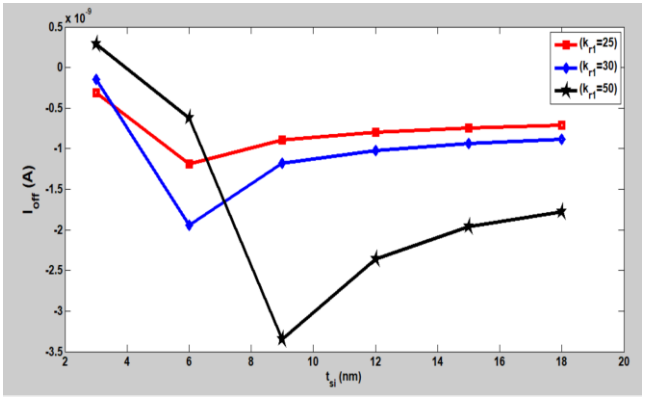

Fig. 4. Variation of off current against t_{si} for different dielectric strength in region I.

A key parameter for analog IC designers is the transconductance (g_m) which measures the gain of the device. Generally, g_m value increases with increase in gate-source voltage due to increased current capability of the device. The proposed Hetero-dielectric gate TFET results in larger g_m compared to the conventional TFET after certain gate bias voltage as seen from Fig. 5(a). This is due to lower subthreshold swing of the proposed structure than the conventional TFET devices. Larger drain voltage results in larger transconductance value (in Fig. 5(b)) due to lower ambipolar current in the proposed structure at any given gate bias voltage.

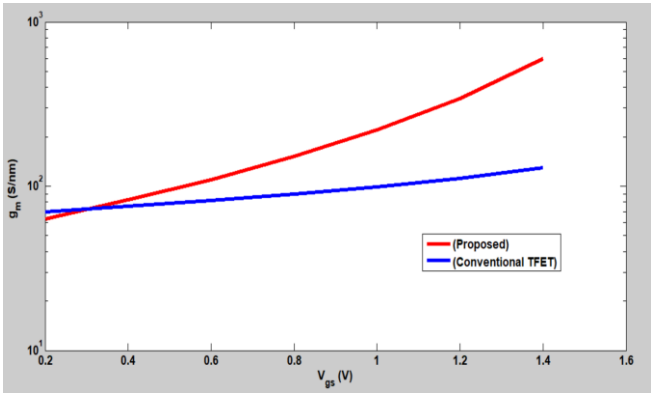

Fig. 5(a). Comparison of g_m value of HDG TFET device with single gate TFET.

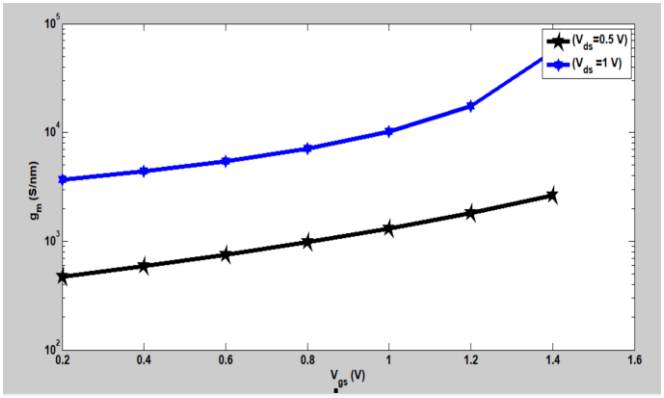

Fig. 5(b). g_m versus V_{gs} for V_{ds} = 0.5 V and 1.0 V.

We have studied the effect of the silicon film thickness on transconductance parameter for two values 10 nm and 15 nm respectively. Figure 6(a) shows that as t_{si} reduces transconductance value increases due to increase in tunneling volume in the channel from source which results larger current drive capability in the device.

The larger g_m results for the case when the region I has lower oxide thickness compared to the ambipolar region as observed from Fig. 6(b). This is due to fact that lower oxide thickness results in larger capacitive effect which enhances the overall drive current of the proposed device.

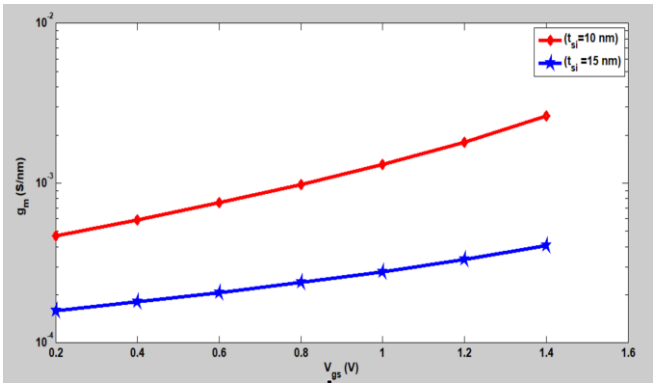

Fig. 6(a). Variation of g_m against V_{gs} for two different values of t_{si}.

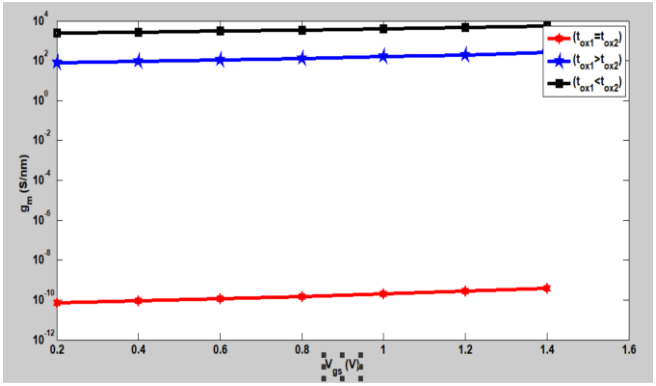

Fig. 6(b). Variation of g_m against V_{gs} for two different combination of oxide thickness.

IV. CONCLUSION

This paper analysed the electrical characteristics of the HDG TFET device. The analytical results of proposed tunneling width models show a good agreement with 2-D ATLAS simulator results. When the whole channel region has been equally divide to accommodate the lower and higher dielectric materials the tunneling probability increases. The on current of the device can be increased considerably by reducing the ambipolar current appreciably by choosing gate material of higher work function near the source region. It is observed that a thinner silicon film and larger drain bias result in larger transconductance value. Since, the proposed structure has lower SS which results larger transconductance value compared to the conventional TFET device. One can enhance the transconductance value of the proposed structure using thinner source gate oxide with combination of material engineering.

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